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Two Nominees, One Winner for Best Research Paper at Computer Enigneering Conference

At the 24th International Conference on Field Programmable Logic (FPL), two papers from the University of California, San Diego were nominated for the top award, and one of the papers from the Computer Science and Engineering (CSE) department won for Best Paper. Both papers dealt with hardware acceleration to speed up software tasks ranging from computer vision to reconstructing human genomes.

The top honor went to the authors of a paper on "Hardware Accelerated Novel Optical De Novo Assembly for Large-Scale Genomes." In addition to CSE professor Ryan Kastner and first author Pingfan Meng, a Ph.D. student in Kastner's group whose research focuses on high-throughput, real-time computing systems using heterogeneous hardware accelerators, other co-authors were CSE Ph.D. student Matthew Jacobsen, former visiting scholar Motoki Kimura, and collaborators from BioNano Genomics (Vladimir Dergachev, Thomas Anantharaman and Michael Requa).

UC San Diego computer science and engineering professor Ryan Kastner co-authored three papers at FPL 2014, including the Best Paper award winner.

The winning paper looked at the potential use of a novel optical label-based technology to make reliable, large-scale de novo assembly of human genomes possible. The new technology requires a more computationally intensive alignment algorithm if it is going to be used reliably for reconstructing large-scale structures such as a human genome.

The run-time of reconstructing a human genome is approximately 10,000 hours on a standard central processing unit (CPU), so the authors looked at three rival approaches to hardware-based acceleration: multi-core CPU; a graphics processing unit (GPU); and field-programmable

gate array (FPGA), which is an integrated circuit that can be customized to different specific use cases.

The new approaches had the desired effect of speeding up the reconstruction of human genomes. The multi-core CPU design was 8.4 times faster; the speedup with GPU was 13.6 times; and by far the greatest acceleration was produced using the FPGA approach, which was 115 times faster that today's sequential CPU approach.

Computer science Ph.D. student Pingfan Meng studies high-throughput, real-time computing systems using heterogeneous hardware accelerators.

FPGA acceleration was also the subject of the second paper from the Kastner group to receive a best-paper nomination at FPL. The paper explored "Improving FPGA Accelerated Tracking with Multiple Online Trained Classifiers." It was co-authored by Ph.D. student Matt Jacobsen, former Kastner group undergraduate Siddarth Sampangi (now a grad student at the University of Massachusetts at Amherst), and CSE professors Yoav Freund and Ryan Kastner. (Both faculty members are academic participants in the Qualcomm Institute at UC San Diego.) In their paper, Jacobsen and his co-authors proposed an FPGA-accelerated design of an online boosting algorithm that used multiple classifiers to track and recover objects in real time – even if their appearance might be changing (e.g., a car and its shadow will look different depending on the time of day and amount of sunlight). The algorithm used a novel method for training and comparing pose-specific classifiers along with adaptive tracking classifiers. The FPGA accelerated design was able to track at 60 frames per second while concurrently evaluating 11 classifiers. This represents a 30-times speed-up over a CPU-based software implementation. The researchers also demonstrated state-of-the-art tracking accuracy on a standard set of videos.

Computer science Ph.D. student Matthew Jacobsen co-authored both best-paper nominees at the FPL 2014 conference.

A third paper from the Kastner group was accepted to FPL 2014. Kastner and his Ph.D. students Dajung Lee (ECE) and Janarbek Matai (CSE) as well as Brad Weals of Toyon Research, reported on “High Throughput Channel Tracking for JTRS Wireless Channel Emulation.”

FPL is the largest conference covering the rapidly growing area of field-programmable logic, and the 2014 conference took place September 2-4 in Munich, Germany.

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